

This Page Is Inserted by IFW Operations  
and is not a part of the Official Record

## **BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

**IMAGES ARE BEST AVAILABLE COPY.**

As rescanning documents *will not* correct images,  
please do not report the images to the  
Image Problem Mailbox.

# PATENT ABSTRACTS OF JAPAN

(11)Publication number : 05-257164

(43)Date of publication of application : 08.10.1993

(51)Int.Cl.

G02F 1/136  
G02F 1/1335

(21)Application number : 04-051817

(71)Applicant : SHARP CORP

(22)Date of filing : 10.03.1992

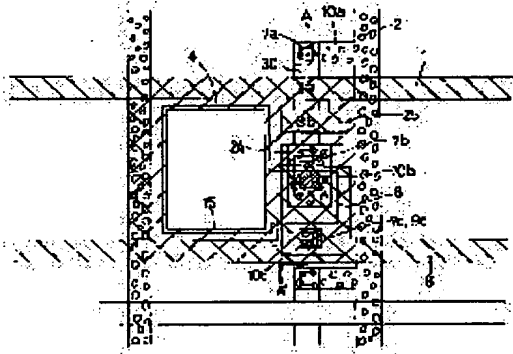
(72)Inventor : MATSUSHIMA YASUHIRO  
SHIMADA NAOYUKI  
YAMASHITA TOSHIHIRO

## (54) ACTIVE MATRIX SUBSTRATE

### (57)Abstract:

**PURPOSE:** To suppress the generation of a signal delay by adopting the circuitry in which a light shielding film and additive capacity common wiring are connected in parallel.

**CONSTITUTION:** Metallic layers 10a to 10c are respectively so formed as to embed contact holes 7a to 7c and are connected to a source electrode, a drain electrode 24 and the additive capacity common wiring 8. The light shielding film 15 is so patterned and formed as to embed the contact hole 9c in addition to the upper part of a thin-film transistor (TFT) 25. The light shielding film 15 constituted in such a manner and the additive capacity common wiring 8 are formed in parallel. The light shielding film 15 and the additive capacity common wiring 8 are electrically connected via the contact holes 7c, 9c respectively provided in first and second interlayer insulating films. Then, the circuitry in which the light shielding film 15 and the additive capacity common wiring 8 are connected in parallel is obtd. and the resistance is lowered, by which the generation of the signal delay is suppressed.



## LEGAL STATUS

[Date of request for examination] 26.01.1996

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number] 2800956

[Date of registration] 10.07.1998

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's  
decision of rejection]

[Date of extinction of right]

Copyright (C); 1998,2000 Japan Patent Office

---

**CLAIMS**


---

**[Claim(s)]**

[Claim 1] While having the spacial configuration by which laminating formation of the picture element electrode, shading film, and addition capacity common wiring was carried out through the layer insulation film between each on the substrate Along with the thing of this picture element electrode located in a line with \*\* on the other hand, this shading film has [ a picture element electrode / this addition capacity common wiring ] the planar structure formed, respectively in parallel [ with this shading film ] beltlike in the shape of a matrix. this shading film This addition capacity common wiring, The active-matrix substrate according to claim 1 electrically connected through the contact hole prepared in this layer insulation film.

[Claim 2] The active-matrix substrate according to claim 1 which the aforementioned shading film becomes from W, Ti, Mo, and a Ti-W alloy.

---

**DETAILED DESCRIPTION**


---

**[Detailed Description of the Invention]****[0001]**

[Industrial Application] this invention relates to the manufacture method of the active-matrix substrate used for example,

for an active-matrix liquid crystal display etc.

**[0002]**

[Description of the Prior Art] In recent years, the active-matrix display using liquid crystal etc. as a display medium is studied actively. Especially, the active-matrix type display which used liquid crystal is studied as a flat-surface display, and the efforts are also bearing fruit it steadily. Such active matrix liquid crystal display is constituted by the active-matrix substrate in which a picture element electrode, TFT (TFT), etc. were formed, the opposite substrate in which the counterelectrode was formed, and the liquid crystal layer enclosed while making these counter.

[0003] Especially in the active matrix liquid crystal display (LCD) designed small and with high definition, on the design, since the area of a picture element becomes small, the capacitor capacity formed between a picture element electrode and a counterelectrode becomes small. Therefore, the required problem of it becoming impossible to carry out time maintenance produces a video signal. In addition, the problem that the change of the potential of bus wiring to the potential of a picture element electrode becomes large is also produced. Then, addition capacity is prepared in order to compensate the shortage of capacity of a picture element electrode and a counterelectrode.

[0004] Drawing 4 shows the plan for one picture element of the conventional active-matrix substrate equipped with addition capacity, and drawing 5 is a cross section (cross section in alignment with B-B' in drawing 4) which passes along TFT25 of the active-matrix substrate. The semiconductor layer 30 which consists of polycrystal silicon with which this active-matrix substrate has the channel layers 12a and 12b, the source electrode 23, and the drain electrode 24 on the insulating substrate 11 is formed. Electric resistance is reduced when portions other than channel layer 12a of the semiconductor layer 30 and 12b perform doping by ion-implantation.

[0005] The semiconductor layer 30 is covered, the gate insulator layer 13 is formed on a substrate 11, and the gate electrodes 3a and 3b and the addition capacity electrode 6 which consist of one of polycrystal Si of n+ or p+ are formed on this gate insulator layer 13.

Above-mentioned doping is performed considering these gate electrodes 3a and 3b as a mask. Gate electrode 3a consists of a part of gate bus wiring 1 self, as shown in drawing 1, and gate electrode 3b consists of portions which branched from the gate bus wiring 1. The addition capacity electrode 6 is a part of addition capacity common wiring 8 which carried out band-like, as shown in drawing 1, and addition capacity is formed in the

opposite portion of the addition capacity common wiring 8 and the picture element electrode 4.

[0006] Furthermore, the gate electrodes 3a and 3b are covered, and the insulator layer 14 is formed between the 1st layer the whole surface on a substrate 11. Through holes 7a and 7b are formed in the insulator layer 14 between the 1st layer. On through hole 7a, metal layer 10a which branched from the source bus wiring 2 is formed. Furthermore, with branched metal layer 10a, metal layer 10b formed simultaneously independently exists. The source bus wiring 2 is connected to the source electrode 23 of TFT25 through through hole 7a. Here, the structure where TFT25 is called dual gate which has the gate electrodes 3a and 3b is used. One contact hole 7b is buried using metals, such as aluminum, in order to perform certainly electrical installation between the drain electrode 24 of TFT25, and metal layer 10b.

[0007] Moreover, an insulator layer 17, the shading film 15, the 3rd layer insulation film 18, and the picture element electrode 4 are formed in this order between the 2nd layer. The shading film 15 and the aforementioned metal layer 10b are connected through contact hole 9b prepared in the insulator layer 17 between the 2nd layer. The shading film 15 is formed with a Ti-W alloy etc. This shading film 15 is also bearing the role

which makes the ohmic contact between metals, such as aluminum which buries contact hole 7b, and the picture element electrode 4 which consists of ITO etc. realize. The shading film 15 and the picture element electrode 4 are connected through contact hole 16b formed in the 3rd layer insulation film 18.

[0008]

[Problem(s) to be Solved by the Invention] By the way, conventionally [ this ], since time until this gate bus wiring 1 becomes the beginning with an OFF state by the source bus wiring 2 used as an ON state is fully long after one of the gate bus wiring 1 will be in an ON state in a substrate, the video signal with which the source bus wiring 2 is sent has a margin in the picture element electrode 4 and the addition capacity electrode 6, and is written in them. However, since time until the gate bus wiring 1 becomes the last with an OFF state by the source bus wiring 2 used as an ON state is short, there is a problem that the write-in time of a video signal is restrained.

[0009] Furthermore, since the addition capacity common wiring 8 is formed by the polycrystal Si of n+, it cannot be said that resistance is small enough.

Therefore, the signal with which the addition capacity common wiring 8 is sent is delayed, and also has the problem that change is caused in the potential with which the \*\*\*\* was restrained and which wrote in, and it becomes

impossible to have written in the video signal in time, and was written in the picture element electrode 4. This problem is explained based on drawing 6.

[0010] Drawing 6 shows the representative circuit schematic of one picture element portion. Between the counterelectrodes 34 to which the picture element electrode 33 connected to the drain electrode 32 of TFT31 and this picture element electrode 33 were countered, and counterelectrode wiring was connected, capacity CLC is formed on both sides of a liquid crystal layer.

Moreover, the drain electrode 32 of TFT31 is connected to addition capacity common wiring through the addition capacity CS. Furthermore, capacity Cgd is formed between the gate electrode 35 of TFT31, and the drain electrode 32.

[0011] If the signal of gate-on is sent to gate bus wiring of TFT at this time, TFT will be in an ON state and a video signal Vd will be written in source bus wiring. Here, if the time constant of the signal transduction of addition capacity common wiring is made into the signal write-in time TON to tauCS and a picture element electrode, when the conditions of  $\tau_{CS} \ll T_{ON}$  will not be fulfilled, charging to the addition capacity CS becomes inadequate, and the problem of changing the potential of a picture element electrode arises.

[0012] By the way, TFT will be in an OFF state and potential Vd' of the picture

element electrode corresponding to the actual display state after passing time long enough compared with  $\tau_{CS}$  is expressed with the one following formula.

[0013]

$$C_{gd}/(C_{gd}+CLC+CS) \text{ and } V_d' = V_d \cdot \{V_g\} \cdot a \quad \text{-- (1)}$$

Here,  $\Delta V_g$  is the difference of the gate potential at the time of the ON state of TFT, and the gate potential at the time of an OFF state.  $a$  expresses change of the potential produced since addition capacity cannot be enough charged within write-in time, and is shown by the two following formulas.

[0014]

$$a = V_d \cdot \exp(-T_{on}/\tau_{CS}) - \{CS/(C_{gd}+CLC+CS)\} \quad \text{-- (2)}$$

The 2nd term in the one above-mentioned formula expresses change of the potential of the picture element electrode by changing the voltage of gate bus wiring, in order to make TFT into an OFF state. In order to make the written-in video signal perform a faithful display, you have to make small the 2nd term of one formula, and the value of  $a$  of two formulas. It is  $C_{gd} \ll CLC+CS$  in order to make the value of the 2nd term of one formula small. -- (3)

\*\*\*\*\* -- things are required In a high definition active-matrix substrate, since a picture element electrode is small and CLC is small, the addition capacity CS of a certain amount of size is needed for fulfilling the conditions of three

formulas.

[0015] Thus, the addition capacity CS is  $T_{on} \ll \tau_{CS}$ , in order to make the value of  $a$  small, since the size of a certain grade is required. -- (4)

\*\*\*\*\* -- things are required

Especially in the small and high definition active-matrix substrate in which the drive circuit was formed on the same substrate as a TFT array, difficulty follows on fulfilling the conditions of the four above-mentioned formula. The reason is shown below.

[0016] \*\* The number of gate bus wiring increases and the time assigned to per-one gate bus wiring becomes short.

[0017] \*\* By the method which mounts a driver IC, although it is satisfactory since a video signal is simultaneously outputted to all source bus wiring, since a video signal is outputted to each source bus wiring one by one when adopting a panel sample hold method, the write-in time in the source bus wiring with which writing is finally performed becomes short.

[0018] \*\* In order to prevent decline in the numerical aperture accompanying highly minute-izing of display, it is necessary to narrow line breadth of wiring. Therefore, resistance of addition capacity common wiring cannot become large, and cannot make  $\tau_{CS}$  small.

[0019] \*\* Even if the number of picture elements increases, the size of the addition capacity common electrode per

one picture element cannot be made small. Therefore, total of the addition capacity connected to addition capacity common wiring of one cannot become large, and cannot make  $\tau_{CS}$  small.

[0020] Although impressing the voltage of a counterelectrode and this potential to the ends of addition capacity common wiring thinks as a solution of such a trouble, since resistance of addition capacity common wiring does not become small enough so then, it cannot be called sufficient solution.

[0021] this invention solves such a trouble, and resistance of wiring which sends a video signal is made small, and it aims at offering the active-matrix substrate which signal delay can be made hard to produce.

[0022]

[Means for Solving the Problem] While the active-matrix substrate of this invention has the spacial configuration by which laminating formation of the picture element electrode, shading film, and addition capacity common wiring was carried out through the layer insulation film between each on the substrate Along with the thing of this picture element electrode located in a line with \*\* on the other hand, this shading film has [ a picture element electrode / this addition capacity common wiring ] the planar structure formed, respectively in parallel [ with this shading film ] beltlike in the shape of a matrix. this

shading film This addition capacity common wiring, It connects electrically through the contact hole prepared in this layer insulation film, and that can attain the above-mentioned purpose.

[0023] You may form the aforementioned shading film with W, Ti, Mo, or a Ti-W alloy.

[0024]

[Function] If it is in this invention, since a shading film and addition capacity common wiring are formed in parallel and a shading film and addition capacity common wiring are electrically connected through the contact hole prepared in the layer insulation film, a shading film and addition capacity common wiring serve as circuitry by which parallel connection was carried out, and resistance becomes small.

[0025]

[Example] The mimetic diagram of active-matrix display is shown in drawing 3.

[0026] As for this display, the gate drive circuit 54, the source drive circuit 55, and the TFT array section 53 are formed on the insulator layer substrates 11, such as glass. The gate bus wiring 1 as the scanning line to which a large number prolonged from the gate drive circuit 54 are parallel is allotted to the TFT array section 53. From the source drive circuit 55, the gate bus wiring 1 and the source bus wiring 2 of a large number as a signal line cross at right angles, and is arranged.

Furthermore, the addition capacity common wiring 8 is arranged in parallel with the source bus wiring 2.

[0027] It is during the gate bus wiring 1 of two, and TFT25, a picture element 57, and the addition capacity 27 are formed in the field of the rectangle inserted with the source bus wiring 2 and the addition capacity common wiring 8. The gate electrode of TFT25 is connected to the gate bus wiring 1, and the source electrode is connected to the source bus wiring 2. Liquid crystal is enclosed between the picture element electrode connected to the drain electrode of TFT25, and the counterelectrode on an opposite substrate, and the picture element 57 is constituted. Moreover, the addition capacity common wiring 8 is connected to the electrode of the same potential as a counterelectrode.

[0028] Drawing 1 shows the plan for one picture element in the active-matrix substrate of this example. Drawing 2 is a cross section in alignment with A-A' in drawing 1. The composition of this active-matrix substrate is explained according to a manufacturing process.

[0029] First, on the insulating substrate 11, after carrying out pattern formation of the semiconductor layer 30 which consists of polycrystal Si by CVD, the gate insulator layer 13 and the becoming insulator layer were formed the whole surface for example, on a substrate 11. This insulator layer is formed by CVD,

the sputtering method, or the method that oxidizes thermally the upper surface of the above-mentioned polycrystal Si thin film 30. The thickness of the gate insulator layer 13 is about 100nm.

Moreover, the thickness of the semiconductor layer 30 is 40-80nm.

[0030] Next, after adhering the polycrystal Si of low resistance, patterning was performed, and the gate bus wiring 1, the gate electrodes 3a and 3b, and the addition capacity common wiring 8 were formed. The addition capacity common wiring 8 contains the addition capacity electrode 6 which is the portion which projected like drawing 1 and was formed. Subsequently, an ion implantation is performed into portions other than the lower part of the gate electrode of the semiconductor layer 30 using the mask which used the above-mentioned gate electrodes 3a and 3b as the mask, and was formed by the photo lithography method. Thereby, the channel layers 12a and 12b are formed in the semiconductor layer 30.

[0031] Then, the insulator layer 14 was formed in the thickness of 700nm between the 1st layer the whole surface on this substrate. Next, contact holes 7a and 7b and contact hole 7c were formed in the predetermined part of an insulator layer 14 between the 1st layer. Each contact holes 7a, 7b, and 7c are arranged after the source electrode 23, the drain electrode 24, and the addition capacity

common wiring 8, respectively.

[0032] Next, the source bus wiring 2, the metal layers 10a, 10b, and 10c, etc. were simultaneously formed using metals of low resistance, such as aluminum. At this time, the metal layers 10a, 10b, and 10c are formed so that contact holes 7a, 7b, and 7c may be buried, respectively, and they are connected with the source electrode 23, the drain electrode 24, and the addition capacity common wiring 8. The thickness of the metal layers 10a, 10b, and 10c which are sticking out on the insulator layer 14 between the 1st layer is 600nm. In addition, metal layer 10a is the portion branched from the source bus wiring 2, and the source bus wiring 2 is connected to the source electrode 23 through metal layer 10a and contact hole 7a.

[0033] Next, the insulator layer 17 was formed in the thickness of 600nm by CVD between the 2nd layer the whole surface on this substrate. Next, contact holes 9b and 9c were formed in the insulator layer 17 between the 2nd layer. Contact hole 9b is for connecting a drain electrode, and contact hole 9c is for connecting the addition capacity common wiring 8 with the shading film 15 electrically.

[0034] Next, pattern formation of the shading film 15 was carried out so that the contact holes 9b and 9c besides the upper part of TFT25 might be buried. Metals, such as for example, a Ti-W alloy, were used for the material of the shading

film 15, and thickness was set to 120-150nm. Although the shading film 15 does not exist in the surroundings of contact hole 9b, since metal layer 10b is formed in this portion, light does not necessarily leak from a portion without the shading film 15. In addition, metals other than an above-mentioned Ti-W alloy, such as W, Ti, and Mo, can be used for the shading film 15. Moreover, the shading film 15 on contact hole 9b is for taking the ohmic contact of the drain electrode 24 and the picture element electrode 4 mentioned later.

[0035] Then, 200nm of 3rd layer insulation film 18 was formed, contact hole 16b was opened and the picture element electrode 4 was formed.

[0036] Therefore, it sets to the active-matrix substrate of this example constituted in this way. Since the shading film 15 and the addition capacity common wiring 8 are formed in parallel and the shading film 15 and the addition capacity common wiring 8 are electrically connected through the 1st and the contact holes 7c and 9c prepared in insulator layers 14 and 17 between the 2nd layer, respectively The shading film 15 and the addition capacity common wiring 8 serve as circuitry by which parallel connection was carried out, and resistance becomes small and can suppress generating of signal delay.

[0037] Moreover, the open circuit produced when line breadth of the

addition capacity common wiring 8 is made thin in order to gather a numerical aperture since the addition capacity common wiring 8 and the shading film 15 had become two-layer structure can be prevented.

[0038]

[Effect of the Invention] As explained in full detail above, a shading film and addition capacity common wiring serve as circuitry by which parallel connection was carried out, resistance becomes small and the active-matrix substrate of this invention can suppress generating of signal delay. Moreover, since addition capacity common wiring and the shading film have two-layer structure, where an open circuit is prevented, the line breadth of addition capacity common wiring can be made small, and profit and the high definition display which has by this the bright screen where a numerical aperture is large can be offered.

---

#### DESCRIPTION OF DRAWINGS

---

[Brief Description of the Drawings]

[Drawing 1] The plan showing one picture element in the active-matrix substrate of this example.

[Drawing 2] The cross section in alignment with A-A' of drawing 1.

[Drawing 3] The mimetic diagram of the active-matrix display equipped with the active-matrix substrate of drawing 1.

[Drawing 4] The plan for one picture

element in the conventional active-matrix substrate.

[Drawing 5] The cross section in alignment with B-B' of drawing 4.

[Drawing 6] The representative circuit schematic of a picture element portion.

[Description of Notations]

1 Gate Bus Wiring

2 Source Bus Wiring

3a, 3b Gate electrode

4 Picture Element Electrode

6 Addition Capacity Electrode

7a, 7b, 7c Contact hole

8 Addition Capacity Common Electrode

9b, 9c Contact hole

10a, 10b, 10c Metal layer

11 Insulating Substrate

12a, 12b Channel layer

13 Gate Insulator Layer

14 Insulator Layer between 1st Layer

15 Shading Film

16b Contact hole

17 Insulator Layer between 2nd Layer

18 Insulator Layer between 3rd Layer

23 Source Electrode

24 Drain Electrode

25 TFT

30 Semiconductor Layer